VLNA 70 - Preamplifier for 70cm

by Sam Jewell, G4DDK

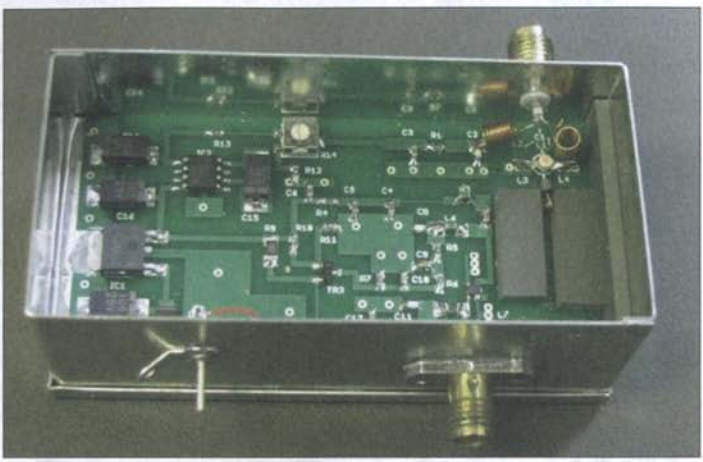

Figure 1: VLNA70

Introduction

My initial attempts to retune a VLNA to work on 70cm were not too successful. Although the modified VLNA would provide an exceptionally low noise figure between 430 and 440MHz, stability was a problem unless the preamplifier was reasonably accurately terminated in 50Ω.

When you consider that the VLNA was originally designed for 23cm, with several of the matching components etched onto the PCB, it is amazing that it is still able to provide a very low noise figure (<0.3dB) at 13cm and <0.4dB at 9cm. However, the massive amount of gain from the two stages together with poor inter-stage matching, at 70cm, meant it was likely to be unstable as configured. However, work to improve the performance of the 23cm version, inspired by RW3BP's results on his 23cm VLNA, opened the way to a solution for the 70cm VLNA stability problems. The 70cm VLNA2+ circuit has now been re-designed to achieve a noise figure down to 0.35dB with careful adjustment. Gain is approximately 40 dB with excellent stability. The input return loss is around 10dB.

Stability has been improved by utilising several techniques. The first and most important is the use of extra source inductance in the first stage. This has had the effect of changing the matching component values and moved the optimum noise matching to a more favourable position on the Smith chart.

A niggling tendency to oscillate at microwave frequencies was cured by the use of the usual absorber material near to TR1 and the use of a ferrite bead on the device drain lead. Gain has been reduced from over 45dB to around 40dB by shunting TR2 drain inductor with a 10R damping resistor. The 70cm preamplifier input has been re-matched to achieve the low noise figure.

The result of this work is that the 70cm VLNA2+ provides a low noise figure with enough stable gain to ensure that an additional second stage preamp is probably no longer necessary in most applications and the buffering effect of TR2 reduces a tendency for mismatches beyond the VLNA to destroy the preamplifier's noise figure due to any poor match reflecting back to the input stage via the previously low S12 figure.

Several lower noise figure preamplifier designs are available in amateur literature. These may be better for your application. The VLNA70 has too much gain (easily reduced by the use of an attenuator after the VLNA) for terrestrial use, as is, and this is reflected in a slightly lower dynamic range than might otherwise be obtainable with some other devices. Do not confuse this with the dynamic range available from single

stage preamps. You often have to add a second gain stage to these in order to get the ultimate noise figure from them, especially for EME. This second stage will inevitably compromise the dynamic range of these preamps.

Circuit description

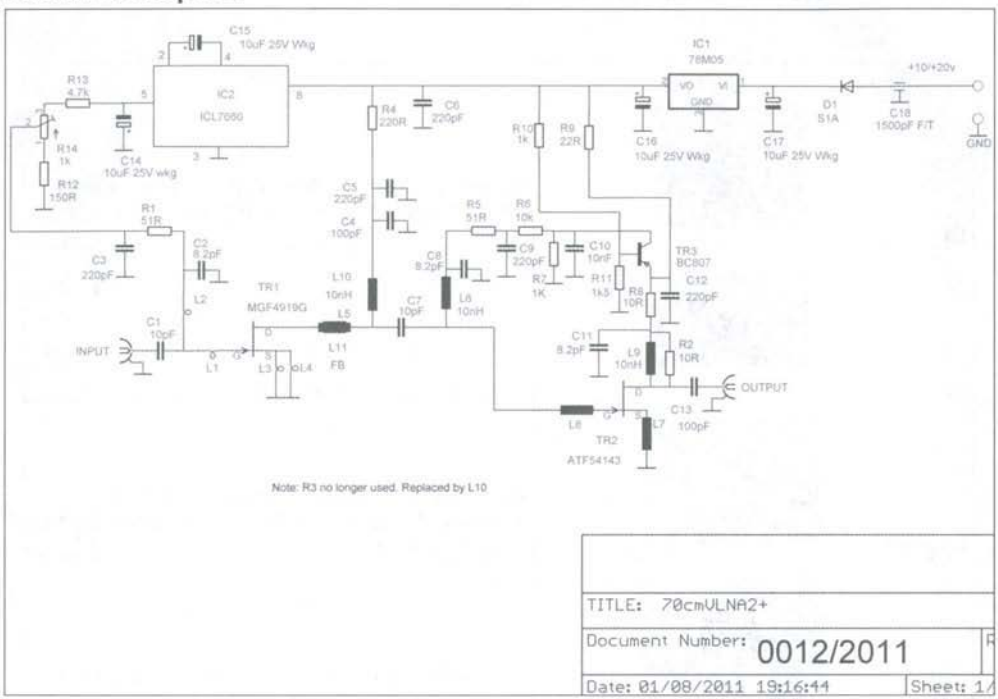

Figure 2: Circuit diagram VLNA70

This follows the usual VLNA schematic except that the input matching component values, together with inter-stage coupling and the all-important TR1 source inductance have been changed to suit the lower frequency.

Starting at the input C1, L1 and L2 provide a low loss noise match such that TR1 'sees' Γopt when looking out towards the 50Ω antenna source impedance. The relatively large amount of source inductance provided by L3 and L4 has the double beneficial effects of improving input return loss as well as frequency stability (as long as there is not too much extra inductance). Any tendency for the low noise stage to produce parasitic oscillations in the GHz region is suppressed by the pieces of absorber material T2, 3 and 4 together with the ferrite bead, FB1. A lot of time was spent trying different ferrite materials and it was found that the specified beads, using Fair-rite 43 material (manufacturers part number 2673000501) worked well. Other materials may also be suitable. TR2 in the 70cm VLNA is identical to the second stage in the 23 and 13cm VLNA amplifiers except that an attempt has been made to reduce the gain a little by shunting L9 with a 10Ω resistor. This can be left out if a few dB more gain is required.

TR1 is biased to approximately 1.5V drain voltage by the gate voltage setting. R14 variable resistor allows the gate voltage to be set such that the drain voltage is 1.5V. This is a starting value and needs to be adjusted on test. It will usually be set close to 1.5V for lowest noise figure. IC2 is the +5V to -5V inverter.

TR2 is an enhancement mode PHEMT and its bias point is set by the active bias circuit comprising TR3 and its associated components. The bias is set so that TR2 drain operates at 3.0 V (2.96V typical) with 60mA drain current. At these values and with the matching used, the dynamic range of this critical second stage is maximised with lowest second stage noise figure.

The VLNA operates internally from 5V provided by the 78M05 500mA regulator. The input voltage to the regulator should be fine up to about 24V as long as C17 has a voltage rating in excess of this. If the supply voltage is taken above 24V then the dissipation in IC1 may be too high unless extra heat sinking is provided. Remember to increase the voltage rating of C17 if you go above 24V.

Construction

The preamplifier must be housed in some form of screened box to prevent unwanted pick up of nearby 433.9MHz Short Range Devices which may, in certain circumstances, saturate the preamplifier. Figure 2 shows the layout of the VLNA70. The dark strips show the position of the ARC10017 absorber tiles. The ferrite bead can be seen on the TR1 drain wire, L5.

Component	Photo	Details
L1		12 turns closewound, 30AWG (0.314mm), Enamel covered copper wire. Inside diameter 2.5mm. 1mm 'tails'
L2		10 turns as L1. 2mm tails
L3 and L4		8mm, wire as L1, bent into hook shape. To be soldered into vias next to TR1. Two required. Before and after shown
L5		8mm, wire as L1. Bent to 'L' shape. Fair-Rite bead slipped over L5 as shown.
T1		42 x 30mm 'tile' of ARC 10017 Absorber material
T2		5mm x 30mm 'tile' of ARC10017 material
T3 and 4		2 x 4mm x 15mm 'tiles' of ARC10017 material

T1 is positioned inside the lid and over the RF section.
It should be approximately 2mm from the end and equally spaced from either side.
T2,3 and 4 should be postioned as shown in the component overlay.

Table 2: VLNA70 Coil and absorber details

Part	Value	Comments	Package
C1	10pF		C-EUC0805
C2, C8, C11	8.2pF		C-EUC0603
C3, C5, C6, C12	220pF		C-EUC0603
C4	100pF		C-EUC0603
C7	10pF		C-EUC0805
C9	1nF		C-EUC0603
C10	10nF		C-EUC0603
C13	100pF		C-EUC0603
C14, C15, C16, 17	10uF 25V		Tantalum
C18	1500pF		Feedthrough
R1, R5	51R		R-EU_R0603
R3		Replaced by L6	
R4	220R		R-EU_R0603
R12	150R		R-EU_R0603
R6	10k		R-EU_R0603
R7, R10	1k		R-EU_R0603
R11	1k5		R-EU_R0603
R14	1k		R-TRIMM
R8	10R		R-EU-R1206
R9	22R		R-EU-R1206
R13	4k7		R-EU-R0603
R15	10R		R-EU-R0603
L1/L2/L3/L4/L5	Length of enamelled covered wire. 0.315mm		See details below.
L6, L9, L10	10nH	L6 replaces R3	SMD0603
FB1	Ferrite bead	Fair-Rite 43 2673000501	2mm x 1.65mm
Tr1	MGF4919	GaAs FET	84
Tr2	ATF54143	GaAs FET	SOT343
Tr3	BC807	PNP transistor	SOT23
IC1	78M05	5V regulator	D-Pak
IC2	ICL7660	DC-DC Converter	SOIC-8
D1	S1A	Protection diode	SMD
CX1, CX2	2 Hole SMA		
T2, T3, T4	Absorber -ARC 10017	One long strip, 2 short	
Box	4 piece tinplate		74mm x 37mm x 30mm
T1	Absorber ARC 10017	Silicone RF absorber tile	30mm x 40mm
PCB	VLNA		72mm x 34mm

Table 1: Component list for the 70cm VLNA2+

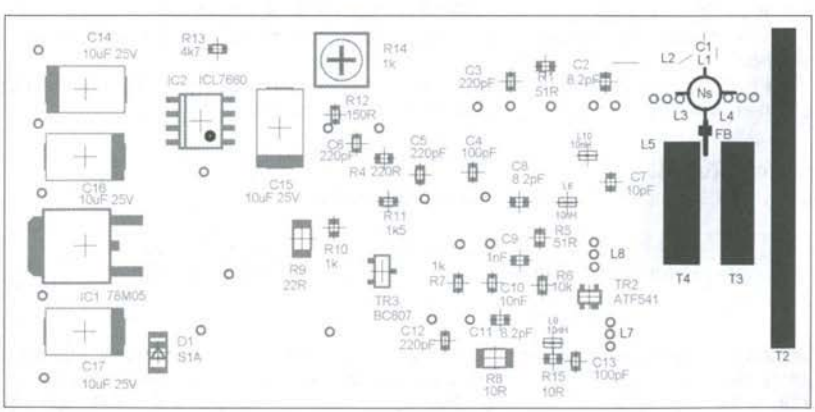

Figure 3: Component overlay VLNA70

Start by removing the notches from the two corners of the PCB to clear the folded edges of the box sides. This is best done with a small file or grinding wheel on a Dremel tool. MAKE SURE YOU REMOVE THE CORRECT CORNERS! Solder all the passive components followed by the ICs and TR2 and 3. Use only 0.5mm diameter solder (or smaller). Cut the TR1 source wires and drain wire to length (all 6mm long). Tin the tails of these wires. Solder the source wires into the holes in the vias next to the white circle marking the position of TR1. The wire should just be level with the ground plane side of the via when correctly inserted. Bend the source wires into 'hooks' as shown in the PDF on my web page and the figure below. Use the small pair of tweezers. The MGF4919 source leads will be soldered to these and the FET will then be about 2mm off the PCB. Solder the L3 and L4 wires no more than 1mm in from the ends of the FET source leads. Solder the drain lead, L5, into place remembering to place the small ferrite bead into the wire before finally soldering to the drain lead. Temporarily solder a wire from C2 to the gate of TR1 to protect it from static damage when soldering the PCB into the box.

Mark the insides of the box as shown in the PDF on my web page. The only difference is that the 4mm hole for the SMA input connector should be 9mm down, rather than 10mm, from the rim of the box. This allows an extra bit of room to accommodate the larger L1. Please be careful not to cut your fingers on the box edges. THEY CAN BE SHARP. Drill the two 4mm holes for the SMA connectors and the 2mm hole for the feed through. The 4mm hole for the input connector should be positioned about 1mm in-board of a line through the gate of TR1. i.e. on the IC2 side of TR1, as well as 9mm down from the box upper rim.

Assemble the box. The PCB should be soldered into the box during this process, as per the PDF on my web page. Its ground plane should be just on the 10mm line. i.e. 10mm up from the lower rim of the box sides. NOTE: solder the side overlap seams INSIDE the box, not outside.

Solder the SMA connectors onto the outside of the box. If you have flush-mounting SMA connectors, use an off-cut of PTFE to centre the SMA in the hole (this is provided in the kit, of course!) Extended PTFE connectors should be prepared, as shown in the PDF, BEFORE soldering to the box.

Solder the feed through into the 2mm hole using the solder tag as the ground connection.

Tin the end of the input SMA and solder the output SMA spill to the output track.

Solder the 10pF 0805 size low ESR capacitor to the input connector spill you have just tinned. Use a small pair of tweezers for this operation. Prepare L1 and L2 and tin their tails. Remove the shorting wire between TR1 gate and C2. Solder L1 and L2 into place. Connect the feed through capacitor between the adjacent track and the feed through with a short piece of insulated wire. That's it. Ready for alignment?

Alignment

There is little to adjust to obtain best performance from the VLNA70.

1. Set R14 to 10% from the counter clockwise position. This will set the drain voltage on TR1 to approximately 1.5 V (as measured from the R4 end of L10 to ground, after the next step).
2. Connect 12V to the input feed through and the ground tag and check that the current taken is approximately 60-70mA. If not, you need to investigate why.
3. Measure TR2 drain voltage as 2.9V +/- 0.1V as measured at the junction of L9, C11 and R8 to ground. The most likely cause of a problem here is due to the 0.6v positive bias not 'getting to' the gate of TR2.
4. Adjust L1 top turn until it is vertical with respect to the remaining turns.

Measure the noise figure and gain with e.g. HP8970A and HP346A noise head. Adjust L1 SLIGHTLY to minimise the noise figure. This will affect both gain and input return loss. This is an iterative process for best performance.

Re-adjust R14 to maximise the gain. This will coincide with lowest noise figure. Do not confuse this with the previous stage where lowest noise figure will NOT occur at the gain peak.

Performance Results

Typical figures from 5 samples of VLNA70 measured at 432MHz:

Noise figure <0.4dB (0.33 - 0.35dB with care)	Gain ~ 39-41dB
Input Return loss ~10dB	Input IP3 ~-12dBm

Table 3

General construction details are give in the VLNA PDF on my home web page www.g4ddk.com (Beware. This is a large document!) Of course a kit is available for the preamplifier. This includes all the parts needed to build the preamplifier including tinplate box, feed through capacitor, PCB, connectors (SMA female only) and all small components. Details are on my web page.